VTC Inc.
Value The Customer™

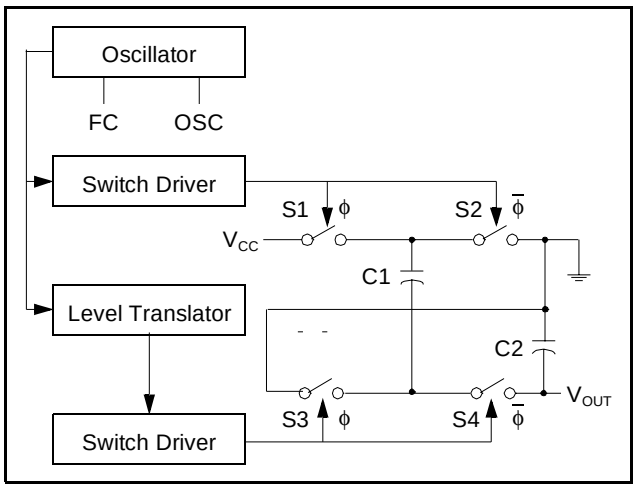
VC4005
+5 VOLT TO -5 VOLT DC VOLTAGE CONVERTER

990823 **ADVANCE INFORMATION** August 23, 1999

FEATURES

- *General*
  - 8 pin SOIC package
  - Inverts input supply voltage (+3V - +5.5V)
  - Very low power dissipation
  - 200mA supply current capability @ R_{OUT} = 3.5Ω
  - High efficiency conversion factor (Typically 85% @ 200mA with V_{IN} = +5.0V)
  - 3Ω typical output resistance
- *Applications*
  - Disk drives utilizing dual-supply preamps
  - Laptop computers
  - Dual supply op-amp power supplies
  - Interface power supplies
  - Medical instruments
  - Cellular phones

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Voltages:
V_{IN} ..... -0.3V to 7V
Junction Temperature ..... 150°C
Storage Temperature, Tstg ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
8-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Input Voltages:
V_{IN} ..... +3V to +5.5V
Switch Capacitors ..... see page 4
Junction Temperature, T_J ..... 25°C to 125°C

CIRCUIT OPERATION

The VC4005 is a high efficiency, switched capacitor voltage converter which inverts the voltage on V_{IN} (+3V to +5.5V) to V_{OUT}. It is capable of 200mA of supply current for applications requiring higher than standard currents such as dual supply preamps for hard disk drives. The VC4005 is also suitable for other dual supply applications such as those listed above. The VC4005 is available with various switch frequencies to best suit the application

Operational Mode

The VC4005 contains four large CMOS switches (S1 - S4) which invert the input supply voltage by switching in a specific sequence. Energy transfer and storage are provided by external capacitors as shown in “Typical Applications” on page 3.

The voltage conversion sequence has two distinct steps:

1) When S1 and S3 are closed, C1 charges to supply voltage V+. S2 and S4 are open during this time interval.
2) When S2 and S4 are closed, C1 charges C2. S1 and S3 are open during this time interval

After several cycles, the voltage across C2 rises to V+.

The output at the cathode of C2 equals -(V+) because the anode of C2 is connected to ground (assuming no load on C2, no loss in the switches, and no ESR in the capacitors). The charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the equivalent series resistance (ESR) of the capacitors.

PIN FUNCTION LIST AND DESCRIPTION

NAME	*I/O*	*DESCRIPTION*
V_{IN}	I	Input voltage to be inverted.
V_{OUT}	O	Output voltage (C2 positive connection)
FC	I	Frequency control: • FC = open, f_{OSC} = 200 kHz. • FC = +V, f_{OSC} = 400 kHz. • FC has no effect when OSC pin is driven externally. • FC must be tied either high or low during operation
CAP +	I/O	C1 positive connection
GND		Power ground
CAP -	I/O	C1 negative connection
OSC	I	Oscillator control input: • Internal 15 pF capacitor. • Connect an external capacitor to ground to lower switching frequency. • Drive with external oscillator to adjust switching frequency.
LV	I	Logic ground

POWER CONTROL PRODUCTS

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	R_L = 1KΩ	3.0	5.0	5.5	V
Power Supply Power Dissipation		Operational Mode		56	**TBD**	mW
Supply Current	I_Q	No Load		3.5	11	mA
Input High Voltage	V_{IH}		2		V_{CC} +0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = V_{IN}$			80	µA
Input Low Current	I_{IL}	V_{IL} = 0 V	-160			µA

NORMAL OPERATION CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

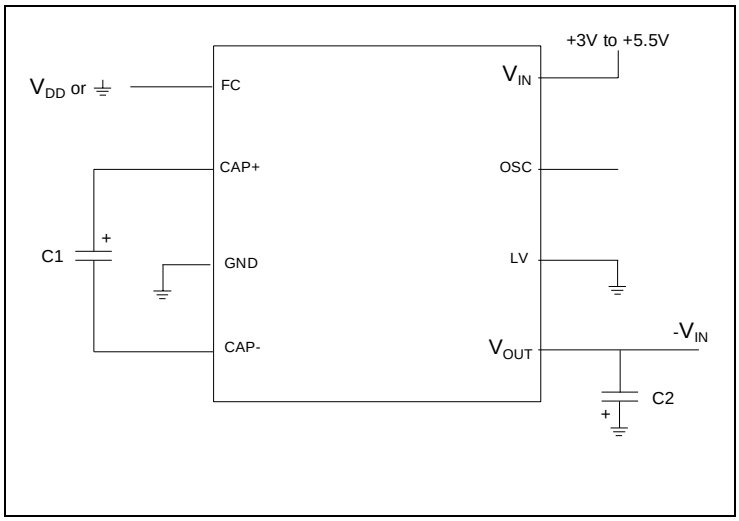
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Output Resistance	R_{OUT}[1]	I_L = 200 mA		3.5	8	Ω
Output Current	I_O	$V_{OUT} \geq -V_{IN}$	200			mA
Oscillator Frequency	F_{OSC}	OSC open, FC = GND	TBD	200		KHz
		OSC open, FC = $+V_{IN}$	TBD	400		
Oscillator Input Current	I_{OSC}	f = 200 kHZ	TBD	+15		µA
		f = 400 kHz	TBD	±30		
Power Efficiency	P_{EFF}	R_L = 500Ω between +V and OUT I_L = 200mA to GND V_{IN} = +5.0 V	TBD TBD	96 86		%
Voltage Conversion Efficiency	V_{CEFF}	No Load	TBD	99		%

1. R_{OUT} includes internal switch resistance and capacitor ESR.

POWER CONTROL PRODUCTS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

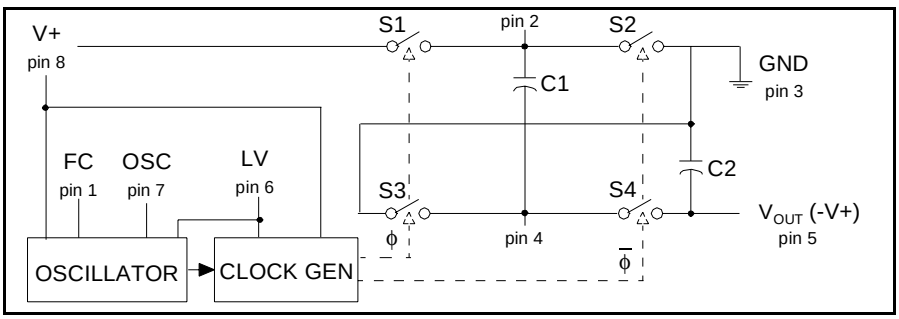
TYPICAL APPLICATION CONNECTIONS



The approximate output of this circuit can be characterized as an ideal voltage source in series with a resistor. The voltage source equals -(V+). The output resistance R_{OUT} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C1 and C2. Since the switching current charging and discharging C1 is approximately twice the output current, the effect of the ESR of the pumping capacitor C1 is multiplied by four in the output resistance. The output capacitor C2 is charging and discharging at a current approximately equal to the output current, therefore its ESR only counts once in the output resistance. A mathematical approximation is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2}$$

Note: R_{SW} is the sum of the ON resistance of the internal MOS switches shown below.



High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the 2/(f_{OSC} x C1) term. Once this term is trivial compared with R_{SW} and the ESRs, further increase of the oscillator frequency and capacitance becomes ineffective.

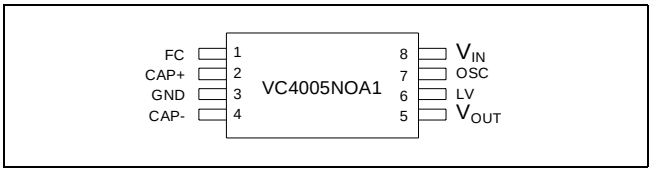
The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C2.

$$V_{ripple} = \frac{I_{Load}}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2}$$

Note: Use of a low ESR capacitor reduces voltage ripple.

PIN ASSIGNMENTS

VC4005 8-lead SOIC



Specific Characteristics

See the general data sheet for common specification information.

NOTES

1) To achieve maximum frequency (400/200 KHz) minimize parasitic capacitance on the oscillator input by *not* bonding-out the oscillator pin.
2) To turn off the converter, drive the oscillator pin to GND or V_{CC}.
3) Use of 10µF, low equivalent series resistance (ESR) capacitors are suggested for C1 and C2. Suppliers/products include:

Supplier [1]	***Part No.***	***Type***	***Value***
Murata	GRM230 Y5V 475 Z16	Ceramic	4.7 µF
	GRM235 Y5V 685 Z16		6.8 µF
	GRM235 Y5V 106 Z16		10.0 µF
	GRM235 Y5V 226 Z10		22.0 µF
Taiyo Yuden	LMK316 BJ 335 ML	Ceramic	3.3 µF
	LMK316 BJ 475 ML		4.7 µF
	JMK316 BJ 106 ML		10.0 µF
	LMK325 F 226 ZN		22.0 µF
AVX	TPSC226 * 016 # 0375	Tantalum	22.0 µF
	TPSC336 * 016 # 0300		33.0 µF
	TPSC476 * 016 # 0350		47.0 µF
	TPSC476 * 016 # 0250		47.0 µF
Sprague	593D335X 035C20	Tantalum	3.3 µF
	593D475X 035C20		4.7 µF
	593D685X 035C20		6.8 µF
	593D106X 035C20		10.0 µF
	593D226X 035C20		22.0 µF
	593D476X 010C20		47.0 µF

1. Supplier telephone numbers are: Murata 800-831-9172, Taiyo Yuden 800-348-2496, AVX 803-448-9411, Sprague 207-324-414.

For best performance, place the capacitors as close as possible to the VC4005. The resistance of the printed circuit board (PCB) will add to the ESR of the capacitors, which reduces the output voltage and efficiency of the VC4005.

4) The test circuit contains capacitors C1 (**TBD**µF) and C2 (**TBD**µF) and ESR (**TBD**). Capacitors with higher ESR will increase the output resistance, which decreases the output voltage and efficiency of the VC4005.