VTC Inc.
Value The Customer™

VM5131

MAGNETO-RESISTIVE HEAD, PROGRAMMABLE READ/WRITE PREAMPLIFIER with SERVO WRITE

990823 **PRELIMINARY** August 23, 1999

FEATURES

- *General*
  - Designed for Use With Four-Terminal MR/GMR Heads
  - 3-Line Serial Interface
    (Provides Programmable Bias Current, Write Current, Head Selection, Thermal Asperity, and Servo Operation)
  - Operates from +8 and +5 Volt Power Supplies
  - 2.5/3.3V CMOS Compatible Logic Interface
  - Fault Detection Capability
  - Available in a 30 or 38-pin VSOP or TSSOP Packages
- *High Performance Reader*
  - Current Bias / Current Sense Architecture
  - MR Bias Current 5-bit DAC, 2 - 9.75 mA Range
  - Programmable Read Voltage Gain
    (112 V/V or 150 V/V typical, 150/190 V/V option available)
  - Thermal Asperity Detection and
    Fast Recovery Compensation
  - Analog and Digital Buffered Head Voltage (ABHV/DBHV) Measurement Modes
  - Input Noise = 0.6 nV/$\sqrt{\text{Hz}}$ Typical
    (R_{MR}=45Ω, I_{MR}=8mA)
  - High Bandwidth = 270 MHz Minimum
    (R_{MR}=45Ω, -3dB)
  - Power Supply Rejection Ratio = (60 dB (1 < f < 100 MHz))
  - Dual Reader Input with One Side Grounded Externally
- *High Speed Writer*
  - Write Current 5-bit DAC, 15 - 60 mA Range
  - Rise Time = 0.8 ns Typical, I_W=40 mA
    (for Real Head Model having L_{TOT}=85 nH)
  - Multi-Channel Servo Write

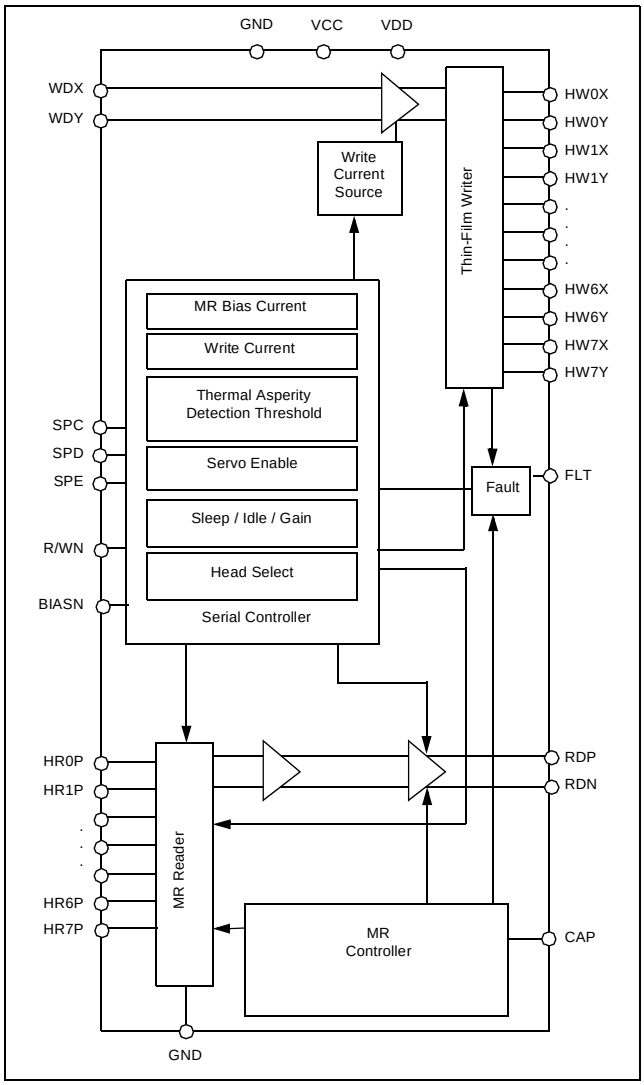
DESCRIPTION

The VM5131 is a high-performance read/write preamplifier designed for use with 4-terminal magneto-resistive recording heads in low-power applications. The VM5131 operates from +8V and +5V power supplies. This device provides write current to the write current drivers, DC bias current for the MR head, read and write fault detection, and multi-channel servo write. This device also provides low voltage power supply detection and power-saving idle and sleep modes.

Programmability of the VM5131 is achieved through a 3-line serial interface. Programmable parameters include MR bias current, write current, head selection, thermal asperity detection threshold and servo operation.

Available as a 4-channel part in a 30-pin TSSOP package or as a 6-channel part in a 38-pin TSSOP package. Please consult VTC for other channel-count and/or package availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V
- V_{DD} ..... -0.3V to +10V

Read Bias Current, I_{MR} 12mA
Write Current, I_W 65mA
Input Voltages:
- Digital Input Voltage, V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage, V_H ..... -0.3V to (V_{CC} + 0.3)V

Output Current:
- RDP, RDN: I_O ..... -10mA

Junction Temperature, T_J ..... 150°C
Storage Temperature, T_{stg} ..... -65° to 150°C
Thermal Characteristics, Θ_{JA}:
- 30-lead VSOP ..... 101°C/W
- 38-lead VSOP ..... 88°C/W
- 48-lead TQFP ..... 75°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%
- V_{DD} .....+8V ± 10%

Write Current, I_W .....15 - 60 mA
Write Head Inductance, L_W ..... 60 - 160 nH
Write Head Resistance, R_W ..... 5 - 25 Ω
Read Bias Current, I_{MR} ..... 2 - 9.75 mA
Read Head Inductance, L_{MR} ..... 20 - 40 nH
Read Head Resistance, R_{MR} ..... 25 - 80 Ω
MR Bias Loop Compensation, CAP ..... 22 nF
Junction Temperature, T_J ..... 0°C to 125°C

OPERATIONAL MODES

Read Mode

In the read mode, the circuit operates as a low noise, single-ended amplifier which senses resistance changes in the MR element that correspond to magnetic field changes on the disk.

The VM5131 uses the current-bias/current-sensing MR architecture. The magnitude of the bias current ranges from 2 - 9.75 mA and is governed by the following equation:

$$I_{MR} = 2 + 0.25(k_{IMR}) \qquad \textit{(eq. 3)}$$

I_{MR} represents the bias current flowing to the MR element (in mA).
k_{IMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>.

A high level signal applied to the R/WN pin and and a low level signal applied to the BIASN pin (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the read mode and activates the read fault detection circuitry (see Table 5).

Passing the magnetic media by the MR element causes MR resistance changes as a result of changes in the magnetic field. The change in resistance is sensed as a change in current within the preamp, and this current change is converted to a differential voltage that is amplified prior to being output to the RDX and RDY pins.

MR Bias Current Enable

Taking the BIASN pin low in read mode enables MR bias current to the selected head.

Taking the BIASN pin high in read mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

The bias current is switched to a 20Ω dummy load during head selection. This allows the bias current to increase from a low bias to the targeted bias current.

Gain and Boost Bits

The GAIN bit (4:<D2>) selects high or low signal gain. The BOOST bit (4:<D4>) increases read gain by 3dB at 80Mhz.

$$A_V = \frac{k}{\frac{25}{I_{MR}} + R_{MR}} \qquad \textit{(eq. 4)}$$

Av represents the Differential Voltage Gain in V/V
Where k = 5390 for low gain or 7219 for high gain.
I_{MR} is in mA.

MR Head Switch Overvoltage Control

The preamp controls the bias current loop capacitor voltage during head switching or modal transitions, in order to prevent overvoltage of the MR element.

When switching between heads, changing I_{MR}, or in any mode where the bias current becomes disabled (Write or Idle modes, or BIASN pin set high in Read mode), the MR bias current is diverted from the MR head while the bias current loop capacitor voltage is quickly discharged to a V_{be} above ground. This ensures that the MR head voltage always rises from a safe voltage to the specific I_{MR}*R_{MR}.

Write Mode

In the write mode, the circuit operates as a thin-film write-current switch, driving the thin-film write element of the MR head.

The magnitude of the write current ranges from 15 - 59.95 mA. The following equation governs the write current magnitude:

$$I_W = 15 + 1.45(k_{IW}) \qquad \textit{(eq. 5)}$$

I_W represents the write current flowing to the selected head (in mA).
k_{IW} represents the write current DAC setting (0 to 31) in 2:<D0-D4>.

A low level applied to R/WN pin (along with the appropriate levels on the IDLEB and SLPB bits) places the preamp in the write mode (see Table 5). The write data signals on the WDX and WDY lines drive the current switch to the thin film writer. Write current polarity is defined in Figure 15.

MR Bias Current Enable

Taking the BIASN pin low in write mode enables MR bias current to the selected head. The read circuitry is in its normal “read” state except that the reader outputs are clamped to maintain their common-mode voltage.

Taking the BIASN pin high in write mode directs the MR bias current to an internal dummy head and common-mode clamps the reader output. The MR bias current source and the MR bias control loop remain active.

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Write Current Waveform Shaping Control

The write current waveform can be shaped using the control bits in register 5. The OSD bit (5:<D1>) selects an increase (OSD = 0) or decrease (OSD = 1) in the amplitude of the overshoot. The OSC bits (5:<D2-D4> select the percentage of overshoot. The USC bits (5:<D5-D7> select the percentage of undershoot.

Note: The overshoot or undershoot induced by the register settings is dependent on write load and current settings. See Tables 9 and 10, and Figures 6 through 9 for examples.

Servo Write Mode

In the servo write mode, the even, odd or all channels of the VM5131 are written simultaneously. The reader circuitry is shutdown during servo mode to reduce power consumption and the associated heat.

MR head fault detection and reporting are disabled during Servo Write Mode.

Servo mode is initiated by a seven-step process (see Table 5):

1) Select Head 0, 2, 3, 4 or 6 (‘none’ in Servo Bank Write).[1]
2) Select Read mode by setting R/WN pin high.
3) Set the SBW0 bit (4:<D5>) to a ’1’.
4) Set the SBW1 bit (2:<D7>) to a ’1’.
5) Set the SBW0 bit to a ’0’ to initiate Servo mode.
6) Select Heads 1, 5 or 7 (‘odd’, ‘all’ or ‘even’ in Servo Bank Write). [2]
7) Set R/WN pin high to enable servo write current. [3]

1. This step prevents an overvoltage spike to the MR heads when servo mode is entered.
2. The HS0-HS2 register bits (1:<D0-D2>) determine which heads are written (see Table 6).
3. R/WN pin enables or disables write current to the heads but does not affect the servo mode.

To exit Servo mode, set SBW1 to ’0’.

Note: The customer is responsible for ensuring that the thermal constraints of the package are not exceeded.
This may be achieved by lowering the supply voltage, reducing the write current, cooling the package or limiting the servo write active duty cycle.
If V_{DD}<7.2V, the LVDIS bit (2:<D6>)must be set to ’1’ in order to continue to write or read.

MR Bias Voltage Enable

Taking the BIASN pin low in servo write mode applies a common voltage bias to all selected heads, see Table 6. The magnitude of this bias voltage ranges from 25 to 226.5 mV and is governed by the following equation:

$$V_{MR} = 25 + 6.5(k_{VMR}) \qquad \textit{(eq. 6)}$$

where V_{MR} represents bias voltage applied to the selected MR element (in mV)
k_{VMR} represents the MR bias DAC setting (0 to 31) in 1:<D3-D7>.

Taking the BIASN pin high in servo write mode disables MR head bias.

MR head fault detection and reporting are disabled during Servo Write mode.

Idle Mode

Setting the IDLEB bit low (4:<D1>) and SLPB bit high (4:<D0>) places the preamp in Idle mode (see Table 5). Only the serial register, bias circuitry and dummy head cell remain active.

The MR bias current source is active and the MR bias current is directed to an internal dummy head. The MR bias current control loop is active and the reader output is clamped at the common-mode voltage.

Sleep Mode

Setting the SLPB bit low (4:<D0>) places the preamp in Sleep mode (see Table 5). All circuits are inactivated to achieve minimal power dissipation. Only the serial register remains active.

Note: Transitions from Sleep mode to Read mode should always be made by first entering the Idle mode for a minimum of 300µs.

Note: After a transition from Sleep mode to Idle mode, the Fault Register (register 6) must be written. This initializes the register to a defined or cleared state.

Table 5 Mode Select

R/WN	*BIASN*	*Servo*	*IDLEB 4:<D1>*	*SLPB 4:<D0>*	*MODE*
1	1	0	1	1	Read Bias Disabled
1	0	0	1	1	Read Bias Enabled
0	1	0	1	1	Write Bias Disabled
0	0	0	1	1	Write Bias Enabled
X	1	1	1	1	Servo [1]
X	0	1	1	1	Servo [1] Bias Enabled
X	X	X	0	1	Idle Bias Disabled
X	X	X	X	0	Sleep

1. Servo Write Mode on page 3 describes the process for initiating.

Table 6 Head Select

HS2 1:<D2>	*HS1 1:<D1>*	*HS0 1:<D0>*	*Normal [1] Write/Read*	*Servo Bank Write*
0	0	0	0	none
0	0	1	1	odd
0	1	0	2	none
0	1	1	3	none
1	0	0	4	none
1	0	1	5	all
1	1	0	6	none
1	1	1	7	even

1. If *Head Selected* > *Channel Count - 1*, an Invalid Head Select fault will be reported.

ESD PROTECTION FOR MR HEAD

Characteristics for ESD diodes at MRP pins are:
R_{ON} = 2Ω, C = 0.3pF, t_{ON} = 0.6ps.

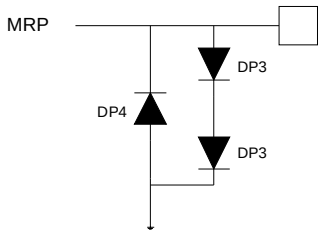

Figure 3 ESD Protection of MR Heads

FAULT HANDLING

Conditions triggering faults, and status and reporting during the fault are listed in Table 7. Non-fault conditions are indicated by a dash, the fault pin level for this condition is that of a safe condition (e.g., Open MR Head in Idle mode, FLT = H).

Table 7 Fault Table

		FLT pin level by Mode [1]					*Register:Bit [2]*
FAULT	***CONDITION***	***Read [3]***	***Write***	***Servo***	***Idle***	***Sleep***	***Setting***
None	Safe	H	L	L	H	H	—
Hot	TEMP bit = 1, Die temperature > 135°C	L	H	H	—	—	6:<D0> = 1
Low V_{CC}	V_{CC} < 3.8V; Resets when V_{CC} > 4.1V	L [4]	H [4,5]	H [5,6]	L	—	—
Low V_{DD}	LVDIS bit = 0, V_{DD} < 6.1V; Resets when V_{DD} > 6.4V	L [4]	H [4,5]	H [5]	L	—	6:<D1> = 1
	LVDIS bit = 1	H	L	L	—	—	6:<D1> = 0
Open MR Head	BIASN pin = L, VMR > 950 mV	L [7]	—	—	—	—	6:<D2> = 1
Shorted MR Head	BIASN pin = L, VMR < 50 mV	L [7]	—	—	—	—	6:<D3> = 1
Invalid Head Select	Head Selected > Channel Count - 1	L [4]	H [6]	—	—	—	—
Open/Shorted Write Head	(ΔV across write element > 2.5V at next WDX/WDY transition, where ΔV = $R_{OpenHead}$*I_W OR Head resistance to GND <15Ω) AND (WDX/WDY transition spacing > Open/Shorted Write Head Blanking Time)	—	H [8]	—	—	—	6:<D4> = 1 6:<D5> = 1
Low Write Frequency	1.5 µs typical between transitions	—	H	—	—	—	6:<D6> = 1
Thermal Asperity	BIASN pin = L, TA DAC > 0, (RDP-RDN) > TA Threshold	L	—	—	—	—	—

1. L = FLT pin low, H = FLT pin high impedance - pulled to level set by external pull-up resistor.
2. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to '0'.
3. Read faults are disabled if MRM is enabled (4:<D3> = 1).
4. MR bias current disabled to MR head. Bias loop capacitor maintained for optimal recovery and at a low voltage to prevent MR element overvoltage.
5. Write current is disabled until the fault is cleared.
6. V_{MR} is not disabled.
7. An open or shorted head fault is latched on the FLT line and the head voltage is clamped to a safe low voltage. The FLT latch and head voltage clamp are cleared by a change in head selection or I_{MR}, or a mode switch.
8. Two WDX/WDY transitions may be required to clear the FLT line after the fault has cleared.

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Other Features Utilizing FLT Pin

Three bits (MRM, ABHV, TEMP) affect the FLT pin output. Table 8 defines the function of the output on the FLT pin.

Table 8 FLT Pin Output Functions

Setting	*Function*	*TEMP 4:<D7>*	*ABHV 4:<D6>*	*MRM 4:<D3>*
1	Normal Fault Reporting [1]	0	0	0
2	DBHV - MR Measurement Mode	0	0	1
3	ABHV - Analog Buffered Head Voltage	0	1	0
4	Not Valid	0	1	1
5	Hot Fault Reporting Enabled (in addition to Normal Fault Reporting)	1	0	0
6	Not Valid	1	0	1
7	Analog Temperature	1	1	0
8	Not Valid	1	1	1

1. As defined in Table 7.

MR Measurement / Digital Buffered Head Voltage (DBHV)

Setting the MRM bit high (4:<D3>) while the TEMP and ABHV bits are low allows the digital buffered head voltage (DBHV) to be represented on the FLT pin.

The FLT output is low when the MR bias current is set to a level that causes the $I_{MR} \cdot R_{MR}$ product to exceed the threshold level as determined by the TA/DBHV DAC (3:<D6-D0>). The FLT output is high when the $I_{MR} \cdot R_{MR}$ product falls below this level.

Note: The FLT line is not valid for 2µs after changing the TA/DBHV DAC.

$$DBHV = 6(k_{TA}) \qquad \textit{(eq. 7)}$$

DBHV represents the voltage level from the MR element (in mV).
k_{TA} represents the TA/DBHV DAC setting (7 to 127) in 3:<D0-D6>.
The threshold settings in TA/DBHV DAC (0 to 6) cannot be detected.

MR Measurement Mode Procedure

Set a fixed IMR bias current and decrease the TA/DBHV DAC settings until the FLT pin goes low. Example: IMR = 6mA, TA/DBHV DAC setting to cause FLT low = 330mV, then MR resistance = 55Ω (330/6).

Analog Buffered Head Voltage (ABHV)

Setting the ABHV bit high (4:<D6>) while the MRM and TEMP bits are low allows an amplified representation of the MR bias voltage to be multiplexed on the FLT pin. (The external pullup resistor must be removed for this mode.) The voltage is defined by the equation:

$$V_{BHV} = 5(I_{MR} \cdot R_{MR}) \qquad \textit{(eq. 8)}$$

Analog Temperature

Setting the ABHV and TEMP bits high while MRM is low multiplexes the voltage representation of the die temperature on the FLT pin. (Note: The external resistor must be removed for this mode of operation.) A voltage (1V to 3V) on the FLT pin represents the die temperature (0°C to 200°C) given by the equation:

$$TEMP(^{o}C) = (V - 1) \times 100 \qquad \textit{(eq. 9)}$$

Where V = voltage (1V to 3V) at FLT pin.

THERMAL ASPERITY DETECTION AND COMPENSATION

A thermal asperity (caused by the collision of the MR element with the media) is characterized by a large amplitude disturbance in the readback signal followed by an exponential decay. The thermal asperity may result in a positive or negative signal disturbance. Figure 4 displays the reader output for an uncompensated, positive thermal asperity event.

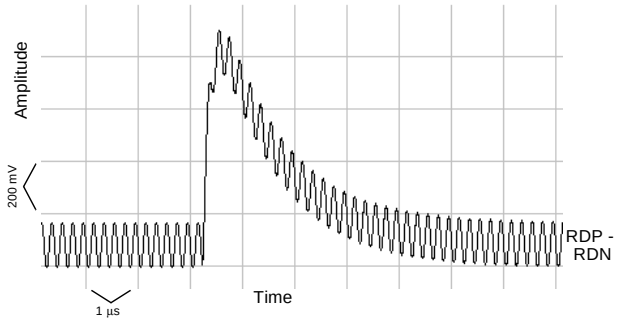

Figure 4 Thermal Asperity Event

Recovery from this large disturbance in the data path can take a relatively large amount of time (typically several microseconds) without detection and correction. The VM5131 implements both a programmable detection threshold and fast recovery compensation for positive, and positive or negative (dual direction) disturbances.

Detection

Programming a non-zero TA detection threshold value (3:<D6-D0>) allows the TA detection circuitry to detect a positive asperity event. Setting the Dual Direction TA bit (7:<D7> = 1) allows detection of positive and negative asperity events. The threshold for thermal asperity detection is output-referred, has a range of 6 - 762 mV and is governed by the following formula:

$$TA_{level} = 6(k_{TA}) \qquad \textit{(eq. 10)}$$

TA_{level} represents the voltage level from the MR element (in mV).
k_{TA} represents the TA DAC setting (1 to 127) in 3:<D0-D6>

TA detection is turned off when the TA detection threshold value is zero (3:<D6-D0> = 0).

Reporting

Whenever a thermal asperity event is detected, it is reported as a low ('0') on the FLT pin.

Compensation and Fast Recovery

When the TAC bit is enabled (3:<D7> = 1), thermal asperity compensation mode is initiated if a thermal asperity is detected.

Note: Setting the TAC bit off (3:<D7> = 0) makes it possible to use the preamp simply as a thermal asperity detector and allow the channel to control the low corner frequency movement.

When activated, Fast Recovery and Compensation raises the nominal 500 KHz lower -3dB corner frequency to approximately 10 MHz until the RDP-RDN output baseline is restored. This adjustment removes the low frequency component of the asperity event and allows the preamp to reach its DC operating point rapidly after a thermal asperity occurrence (ensuring complete output recovery within nanoseconds rather than microseconds; see Figure 5). Additional TA events during t_{D5} will not be compensated.

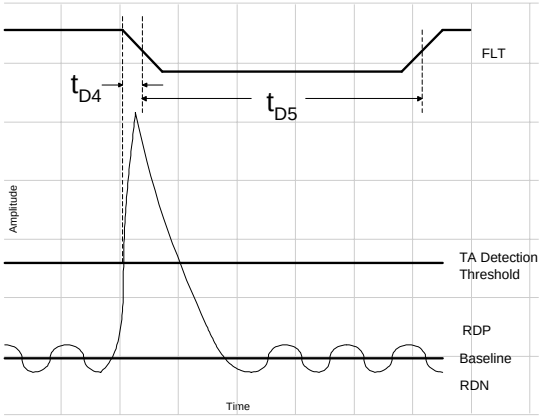

Figure 5 TA Detection and Compensation

After the RDP-RDN output baseline is restored, the preamp reinstates the lower -3dB corner frequency.

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WRITE CURRENT WAVEFORM SHAPING

Tables 9 and 10 summarize write current simulations at both 40 and 60 mA with the load as shown in Figure 6 . The family of curves in Figures 7 through 9 depict the response of programmable overshoot and undershoot under nominal conditions (nominal process, V_{DD} = 8V, V_{CC} = 5V, and T = 75^{o}C). For the calculations of over/undershoot, I_W is the write current amplitude from base (0mA) to the settled point (write current setting in mA). The write current is the current in R2 in the head model depicted in Figure 6.

Table 9 Write Current Overshoot Control

OSD 5:D1	OSC2 5:D4	OSC1 5:D3	OSC0 5:D2	Iw = 40 mA		Iw = 60 mA	
				Overshoot % [1]	% Change from '000' [2]	Overshoot % [1]	% Change from '000' [2]
0	0	0	0	90	0	53	0
0	0	0	1	95	5	57	3
0	0	1	0	103	13	62	8
0	0	1	1	110	20	67	13
0	1	0	0	118	28	70	17
0	1	0	1	128	38	73	20
0	1	1	0	133	43	75	22
0	1	1	1	138	48	77	23
1	0	0	0	90	0	53	0
1	0	0	1	73	-18	45	-8
1	0	1	0	60	-30	40	-13
1	0	1	1	55	-35	37	-17
1	1	0	0	48	-43	30	-23
1	1	0	1	40	-50	25	-28
1	1	1	0	35	-55	20	-33
1	1	1	1	33	-58	17	-37

1. Overshoot % = (Overshoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

Table 10 Write Current Undershoot Control

USC2 5:D7	USC1 5:D6	USC0 5:D5	Iw = 40 mA		Iw = 60 mA	
			Undershoot % [1]	% Change from '000' [2]	Undershoot % [1]	% Change from '000' [2]
0	0	0	-23	0	-18	0
0	0	1	-15	8	-10	8
0	1	0	-10	13	-8	10
0	1	1	-5	18	-7	12
1	0	0	0	23	-5	13
1	0	1	5	28	-3	15
1	1	0	8	30	-2	17
1	1	1	10	33	0	18

1. Undershoot % = (Undershoot/Iw - 1)*100
2. '000' = Natural Response for Iw in R2

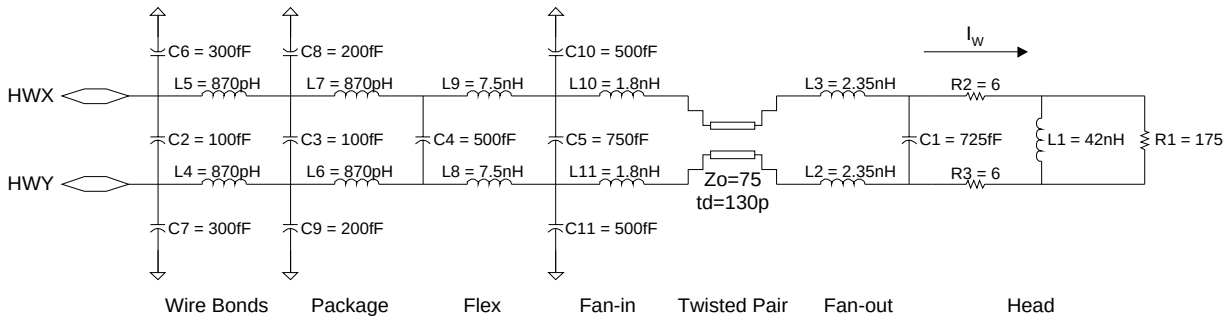

Figure 6 Writer Head Model

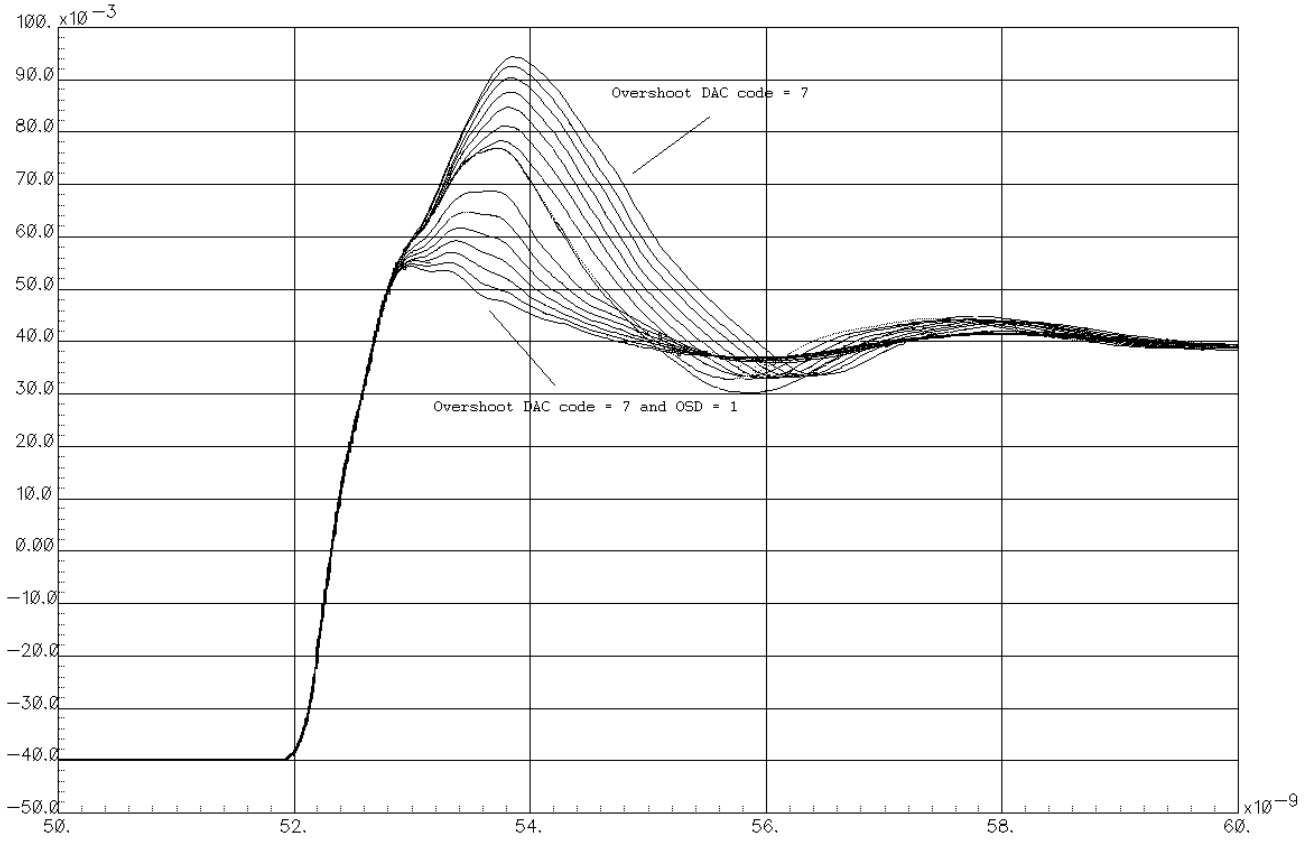

Figure 7 Simulation Of The Programmable Overshoot at Iw=40mA Under Nominal Conditions (nom process, +8,+5V power, 75°C)

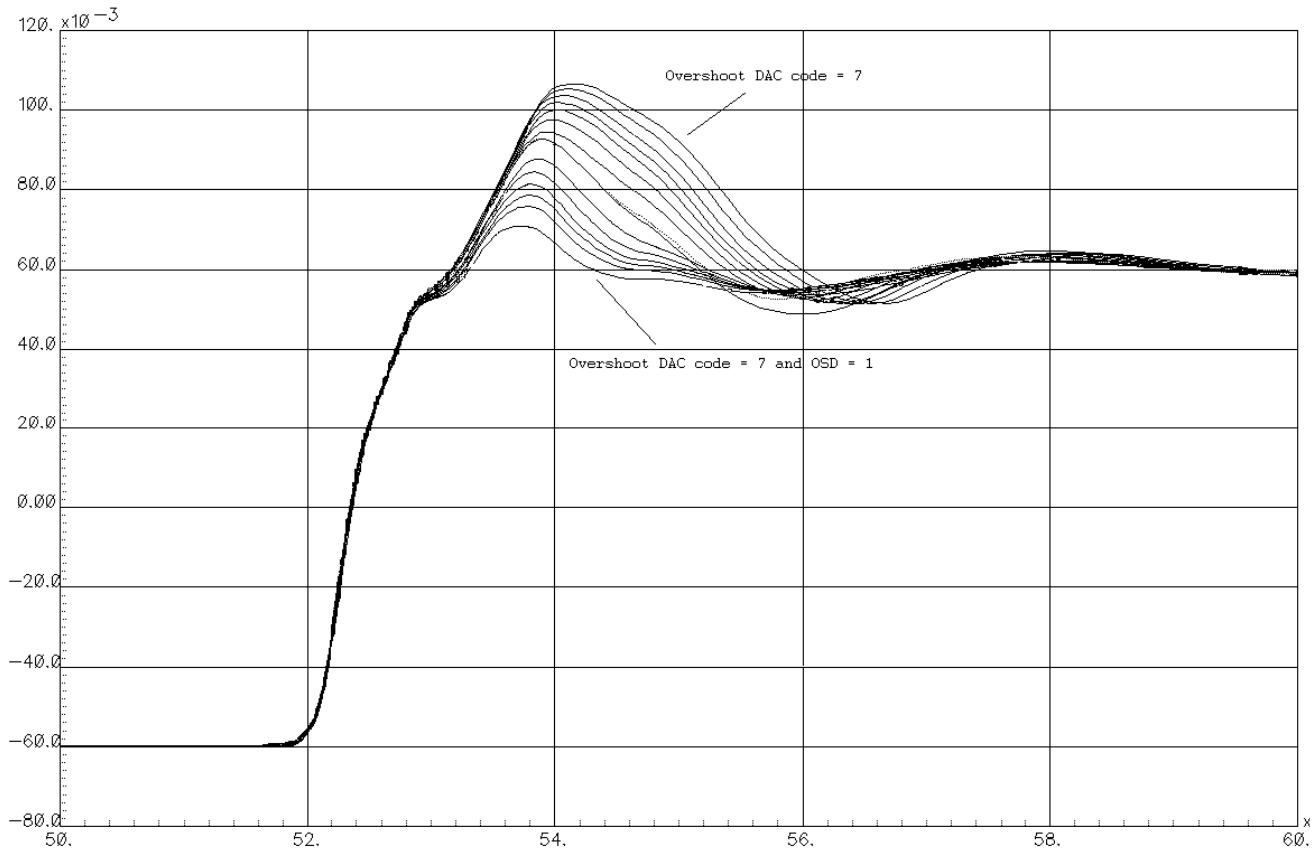

Figure 8 Simulation Of The Programmable Overshoot at Iw=60mA Under Nominal Conditions (nom process, +8,+5V power, 75°C)

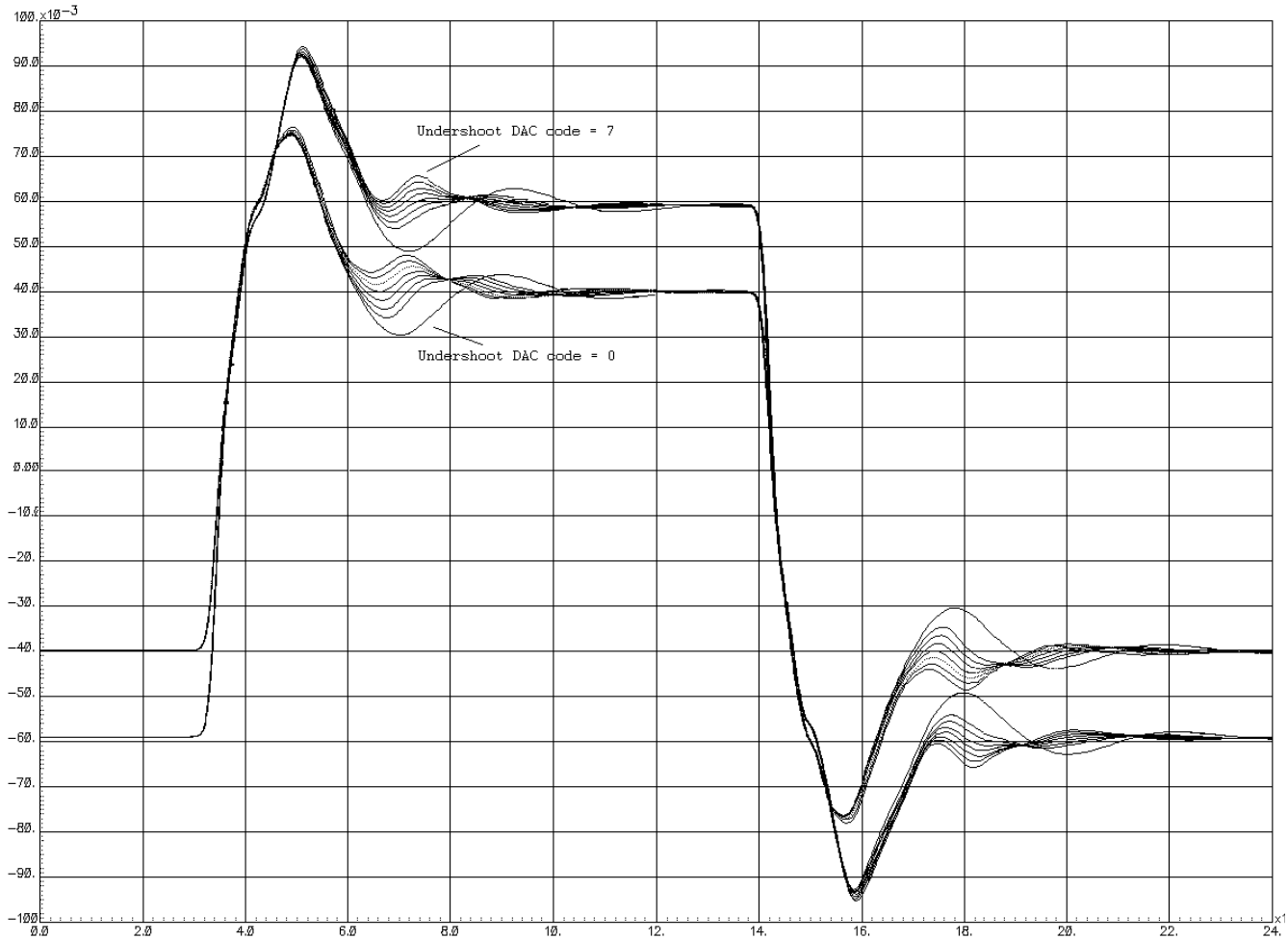

Figure 9 Simulation Of The Programmable Undershoot at Iw=40 and 60mA Under Nominal Conditions (nom process, +8,+5V power, 75°C)

PINNED LAYER REVERSAL MODE

Pinned Layer Reversal (PLR) mode provides a means to correct GMR heads that are affected by a reversed pinned layer. When the preamp is placed in the PLR mode, a positive reset pulse can be applied to the selected head. The external BIASN pin is used to control the timing of the delivery of the reset pulse to the GMR element. Several control bits are provided to shape the reset pulse. These controls include pulse amplitude, duration and decay rate. (See PINNED LAYER REVERSAL CHARACTERISTICS on page 26 for specifications.)

PLR Reset Pulse Controls

The amplitude of the reset pulse ranges from 0.4 to 1.64 V and is governed by the following equation:

$$V_{RESET} = 0.4 + 0.04(k_{PLR}) \qquad \textit{(eq. 11)}$$

where V_{RESET} represents the reset pulse voltage amplitude
k_{PLR} represents the IW DAC setting (0 to 31) in 2:<D0-D4>.
Note that the MR heads ESD diodes may limit the maximum V_{RESET} amplitude achieved to around 1.4V.

The reset pulse duration and decay time are determined by the settings of the PLRPW bits (7:<D2-D3>) as shown in Table 11 and the PLRDT bits (7:<D0-D1>) as shown in Table 12.

Table 11 PLR Reset Pulse Width

PLRPW1 7:<D2>	*PLRPW0 7:<D3>*	*PLR Pulse Width (ns)*
0	0	50
0	1	100
1	0	150
1	1	200

Table 12 PLR Reset Pulse Decay Rate

PLRDT1 7:<D0>	*PLRDT0 7:<D1>*	*PLR Decay Rate (mV/ns)*
0	0	7
0	1	4.67
1	0	2.33
1	1	1.75

PLR Timing and Event Description

Figure 10 depicts a timing diagram for the PLR mode. The steps involved are:

1) Set up VRESET via IW DAC, IMR, PLRPW and PLRDT, and select the head to be reset while in Idle or Read mode.
2) Enter the Read mode by setting IDLEB bit to '1'. Bring BIASN high to disable MR head bias.
3) Enter PLR mode by setting PLREN bit 7:<D4> to '1'.
4) After a minimum time t_{ARM}, bring BIASN low to trigger the pulse.

   Note: The PLR trigger depends on the sequence PLREN set to '1' followed by a high to low transition of the BIASN pin. Subsequent high to low transitions of BIASN will *not* retrigger the PLR mode.

5) Exit the PLR mode after a minimum time t_{EN}, by setting PLREN bit to '0'.
The device returns to Read mode, in which the state of the BIASN pin controls MR head bias.

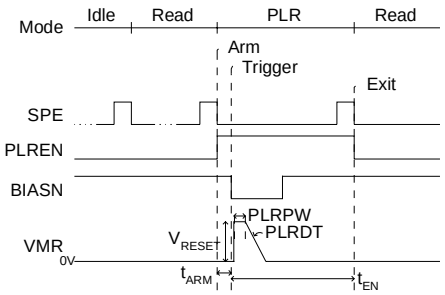

Figure 10 PLR Timing Diagram

VM5131 SERIAL PORT INTERFACE AND CONTROL REGISTERS

The serial port interface and the associated control registers provide programming and monitoring of the VM5131 circuitry. The interface handles the communication between a system control chip and the VM5131 via a three wire interface and related protocols. The control registers hold programming data written to the VM5131 and provide readback monitoring of data held or generated within the VM5131.

Note: If serial port activity is performed during Read mode, crosstalk to the reader output may result.

Serial Port Interface

The serial port interface provides for both writing data to and reading data from the VM5131. Its three pins are:

- SPC (Serial Port Clock) synchronizes the transfer.
- SPD (Serial Port Data) is the bi-directional data pin.
- SPE (Serial Port Enable) enables and disables a serial transfer.

All data writes or reads are enabled by setting SPE = 1 after which the SPC clocks data in or out via the SPD.

Writing to the Serial Port

A data transfer is initiated by setting SPE = '1'. A write data packet is structured as a 16-bit word: '0' for writing + 3 page address bits + 4 byte address bits + 8 programming data bits.

Each rising edge of SPC clocks data into the serial port interface. For valid data transfers, data are loaded into a designated register location upon the falling edge of SPE. Only the first 16 SPC rising edges after SPE goes high are recognized by the serial port interface. Any SPC rising edges after the first 16 are ignored. If less than 16 clock pulses are provided before SPE goes low, the data transfer is aborted.

Figure 11 shows the protocol for a write transfer operation. Refer to Table 13 and Figure 13 for timing specifications for the serial port interface.

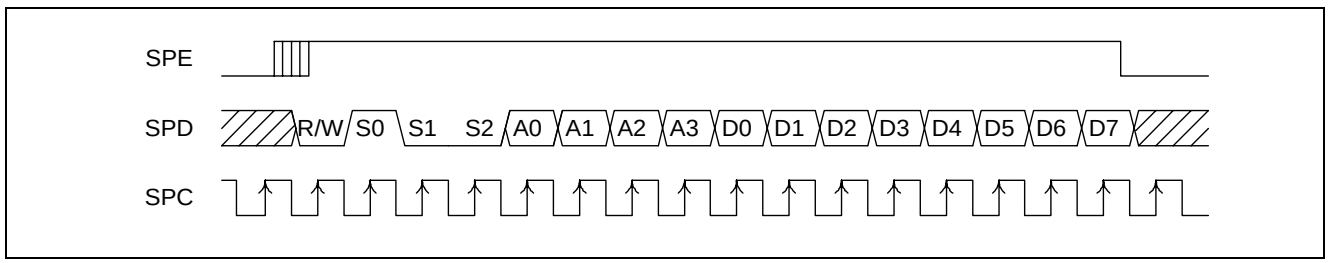

Figure 11 Write Protocol for 3-Write Serial Port Interface

Readback from the Serial Port

The read data packet is structured as: '1' for reading + 3 page address bits + 4 byte address bits + 8 data bits. To perform a read instruction, first set SPE =1 and then input the read instruction bit '1', the 3-bit page address, and the 4-bit byte address. The 8-bits at the specified register address are subsequently clocked out at the SPD pin.

Each rising edge of SPC clocks the instruction bit and the address bits into the serial port interface and the rising SPC edge also clocks out the data information. The SPE falling edge returns the SPD pin to an input pin state. The serial port interface drives the SPD pin only if the page address matches that of the VM5131.

Figure 12 shows the protocol for a read transfer operation. Refer to Table 13 and Figure 13 for timing specifications for the serial port interface.

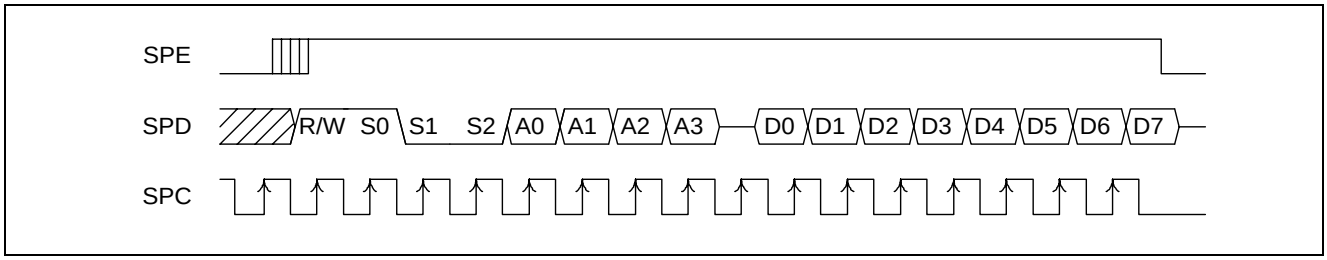

Figure 12 Read Protocol for 3-Wire Serial Port Interface

Table 13 Serial Port Interface Timing Specifications

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SPC Frequency	f_{SPC}	Write operation			25	MHz
		Readback operation			12.5	MHz
SPC High Time	t_{SPCH}	Write operation	14			ns
		Readback operation	32			ns
SPC Low Time	t_{SPCL}	Write operation	14			ns
		Readback operation	32			ns
SPE Rise Setup Time	t_{SEr}	Relative to SPC rising edge	10			ns
SPE Rise Hold Time	t_{HEr}	Relative to SPC rising edge	10			ns
SPE Fall Hold Time	t_{HEf}	Relative to SPC rising edge	10			ns
SPD Setup Time	t_{SD}	Data input relative to SPC rising edge	10			ns
SPD Hold Time	t_{HD}	Data input relative to SPC rising edge	10			ns
SPD Prop Delay	t_{PDD}	Data output relative to SPC rising edge			16	ns
SPD Enable Time	t_{PZD}	Time to take control of SPD relative to SPC rising edge			16	ns
SPD Disable Time	t_{PDZ}	Time to release control of SPD relative to SPE falling edge			16	ns
SPE Low Time	t_{SPEL}	Between transmissions	1/ f_{SPC}			ns

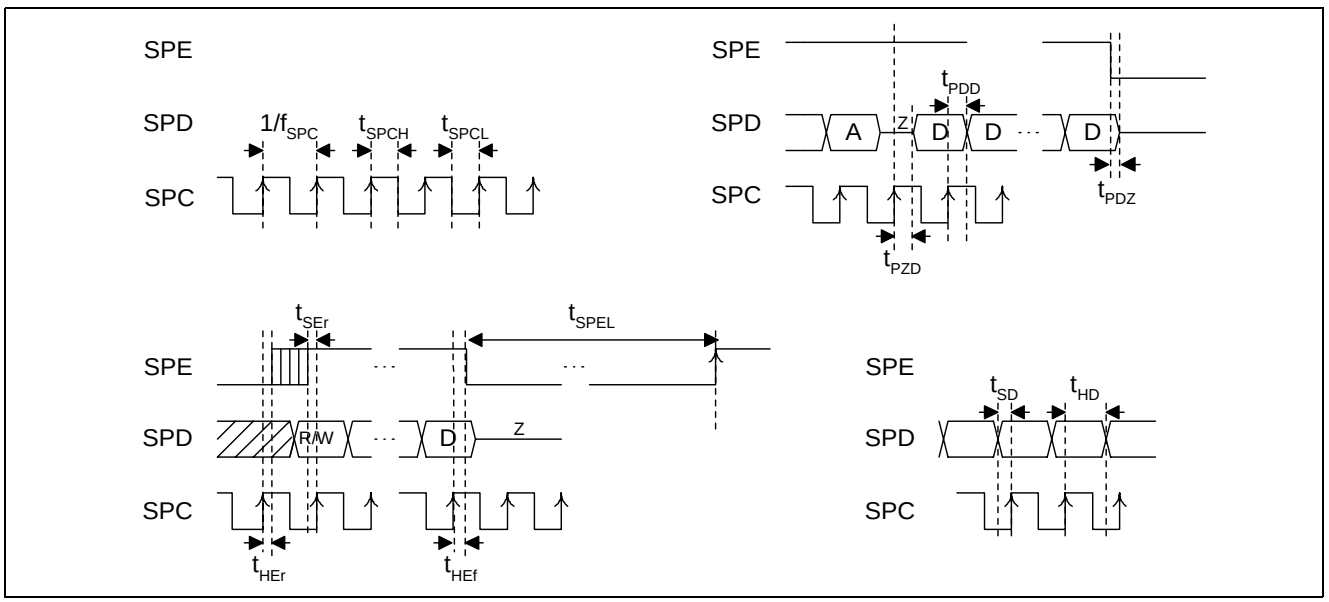

Figure 13 Timing Diagrams for 3-Wire Serial Port Interface

Control Registers

Control registers provide for storage and readback of programming data (i.e., an SRAM type function) and for monitoring of information generated (i.e., SRLatch type function) or hard-coded within the VM5131 (i.e., a ROM type function). The control registers are organized in byte-wide segments, each byte being either an SRAM-type, a ROM-type, or a SRLatch-type.

The addressing scheme for an entire system is as follows. There are 7 bits of address in a system. The first 3 bits, S0-S2, determine the page address, while the last 4 bits, A0-A4, determine a particular byte address within a page. A system may have a total of 8 pages with a total of 16 bytes per page. Each chip in the system is assigned one or more full pages (the VM5131 has a single page). All 16 bytes within each assigned page need not be used. Unused bytes within a chip's page are reserved for possible future use within the assigned chip; they may not be reassigned within the system.

Data written to an unused byte or page address is ignored. Reading from an unused byte in a valid page results in a logic '1' on the SPD line. However, reading from an invalid page address results in no data being transmitted, as the SPD output driver remains turned off until a valid page is addressed. When data is to be read from a valid page address all other chips must keep their SPD output drivers turned off and allow the chip assigned that page address sole control of the SPD line.

VM5131 control registers extend across one page address. The page address is S<0:2> = 1 (001_b) and it contains byte addresses 0 (0000_b) to 15 (1111_b), but not all 16 bytes are used. Table 14 depicts register bit assignments and Table 15 explains the defined register bits. All SRAM and SRLatch registers are set to logic '0' at power-up. Register 0, a ROM type, is hard-coded as follows: the channel count indicator bits (CCI0 to CCI1) are set so that 01_b = 4 channels and 00_b = 6 channels, the revision level bits (REV0 to REV2) are programmed to the appropriate design revision level (0 = 000_b and 7 = $111_{b)}$ and the vendor bits (VEN0 to VEN2) are set to 2 (010_b).

Table 14 Control Register Map

Register			***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0*** [1]
Address	***Title***	***Type***								
0	ID/Rev	ROM	CCI1	CCI0	REV2	REV1	REV0	VEN2	VEN1	VEN0
1	HS/IMR	SRAM	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
2	IW/Servo	SRAM	SBW1	LVDIS	[2]	IW4	IW3	IW2	IW1	IW0
3	TA	SRAM	TAC	TA6	TA5	TA4	TA3	TA2	TA1	TA0
4	Mode	SRAM	TEMP	ABHV	SBW0	BOOST	MRM	GAIN	IDLEB	SLPB
5	WCC	SRAM	USC2	USC1	USC0	OSC2	OSC1	OSC0	OSD	[2]
6	Faults [3]	SRLatch	[2]	LOFR	WRSH	WROP	MRSH	MROP	LOVDD	HOT
7	PLR	SRAM	DUALTA	TOSC	OSDLY	PLREN	PLRPW0	PLRPW1	PLRDT0	PLRDT1

1. <D0> is the first bit written to or read from the register. i.e., LSB first.
2. Reserved
3. See Table 7 for definition of the faults.

Table 15 Control Register Bit Definitions

Register/ Bits	*Bit Name*	*Functional Description*
0:<D0-D2>	VEN<0:2>	Vendor ID of device (read only).
0:<D3-D5>	REV<0:2>	Revision level of device (read only).
0:<D6-D7>	CCI<0:1>	Channel Count Indicator (read only); set to 01_b = 4 channels or 00_b = 6 channels.
1:<D0-D2>	HS<0:2>	Head Select setting. See Table 6 on page 3 for further definition.
1:<D3-D7>	IMR<0:4>	MR head bias current DAC setting (0-31). See Read Mode on page 2 for further definition. In servo write mode, setting determines MR bias voltage as defined in (eq. 6) on page 3.
2:<D0-D4>	IW<0:4>	Write current DAC setting (0-31). See Write Mode on page 2 for further definition. In PLR mode, setting determines PLR amplitude as defined in (eq. 11) on page 11.
2:<D6>	LVDIS	Low V_{DD} disable fault reporting; set to 1 to disable reporting.
4:<D5> 2:<D7>	SBW0 SBW1	Servo Bank Write enable; follow sequence in Servo Write Mode on page 3.
3:<D0-D6>	TA<0:7>	Thermal Asperity Detection DAC setting (1-127) or Digital Buffered Head Voltage DAC setting (7-127). See Detection on page 6 or MR Measurement / Digital Buffered Head Voltage (DBHV) on page 5 for further definition.
3:<D7>	TAC	Thermal Asperity Compensation enable; set to 1 to select.
4:<D0>	SLPB	Sleep mode enable; set to 0 to select.
4:<D1>	IDLEB	Idle mode enable; set to 0 to select.
4:<D2>	GAIN	Gain selection: set to 0 for low gain, set to 1 for high gain.
4:<D3>	MRM	Head Resistance Measurement (DBHV) mode enable; set to 1 to select. See Table 8.
4:<D4>	BOOST	Boost circuit enable; set to 1 to select.
4:<D6>	ABHV	Analog Buffered Head Voltage enable; set to 1 to output ABHV at FLT pin. See Table 8.
4:<D7>	TEMP	Temperature fault report enable; set to 1 to report a temperature fault to the HOT bit and the FLT pin. See Table 8.
5:<D1>	OSD	Write current overshoot direction of control; set to 0 to increase, set to 1 to decrease
5:<D2-D4>	OSC<0:3>	Write current overshoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 7 for further definition.
5:<D5-D7>	USC<0:3>	Write current undershoot correction; See WRITE CURRENT WAVEFORM SHAPING on page 7 for further definition.
6:<D0>	HOT	Bit is set to 1 if the HOT fault occurs. [1]
6:<D1>	LOVDD	Bit is set to 1 if the Low V_{DD} fault occurs. [1]
6:<D2>	MROP	Bit is set to 1 if an MR Open head fault occurs. [1]
6:<D3>	MRSH	Bit is set to 1 if an MR Shorted head fault occurs. [1]
6:<D4> 6:<D5>	WROP WRSH	Bits are set to 1 if a Writer Open head or Head Shorted to ground fault occurs. [1]
6:<D6>	LOFR	Bit is set to 1 if the Write data frequency too low fault occurs. [1]
7:<D0-D1>	PLRDT	PLR Delay Time. See Table 12.
7:<D2-D3>	PLRPW	PLR Pulse Width. See Table 11.

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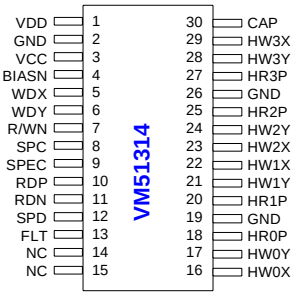
Table 15 Control Register Bit Definitions

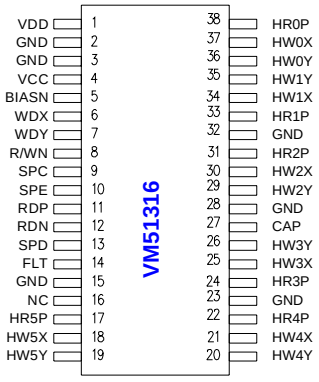
7:<D4>	PLREN	PLR Enable, set to 1 enable PLR mode.
7:<D5>	OSDLY	Additional Write Current Overshoot Control, set to 1 to select.
7:<D6>	TOSC	Manufacturer Test Bit; set to 0 for normal operation.
7:<D7>	DUALTA	Dual Direction TA Detection (positive *and* negative), set to 1 to select.

1. A serial port write to register 6, a SRLatch register, resets all bits in register 6 to '0'.

PIN DESCRIPTION AND FUNCTION LIST



4-Channel
30-lead VSOP (TSSOP)



6-CHANNEL
38VSOP (TSSOP)

Figure 14 Pin Layouts

Table 16 Pin Functions

Signal	*I/O* [1]	*Description*
R/WN	I	Read/WriteNot: Low voltage CMOS input. Internal pull-up resistor (50kΩ). • A low level enables Write mode. • Pin defaults high (Read mode).
BIASN	I	Bias Enable and PLR trigger: Low voltage CMOS input. Internal pull-up resistor (20kΩ) to V_{CC}. • A high level directs bias current to a dummy head. Pin defaults high. • A low level enables MR bias current to the selected head. If PLREN = 1 (7:<D4>), a high to low transition triggers the PLR pulse (V_{MR}). See the PLR Timing and Event Description on page 11.
FLT	O	Fault Status: Open drain output. Requires external pull-up resistor (e.g., 2kΩ to 3V). • In Write mode, a high level indicates a fault. • In Read mode, a low level indicates a fault. • Measurements modes are shown in Table 8 on page 5.
WDX, WDY	I	2V ±100mV write data inputs.
HR0P-HR7P	I	MR head connections, positive end.
HW0X-HW7X	O	Thin-Film write head connections, positive end.
HW0Y-HW7Y	O	Thin-Film write head connections, negative end.
RDP, RDN	O	Read Data: Differential read signal outputs.
CAP	-	Compensation capacitor (22nF) for the MR bias current loop.
GND	-	Ground and common return for MR heads
VCC	-	+5.0V supply
VDD	-	+8.0V supply
SPE	I	Serial Enable: Low voltage CMOS input; see Figures 13 and 15.

Table 16 Pin Functions

Signal	*I/O* [1]	*Description*
SPC	I	Serial Clock: Low voltage CMOS input; see Figures 13 and 15.
SPD	I/O	Serial Data: Low voltage CMOS input/output; see Figures 13 and 15. Requires external pull-up resistor (e.g., 1kΩ to 3V).

1. I = Input pin, O = Output pin.

POWER CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_{MR}=8 mA, I_W=40.0 mA, I_S=25mA.
Power supply currents for other settings can be calculated using the formulas below.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		7.2	8	8.8	V
V_{DD} Power Supply Current	I_{DD}	Read Mode (See Formula 1 below.)		27	31	mA
		Read Mode, Bias disabled		16	20	
		Write Mode (See Formula 2 below.)		72	82	
		Write Mode, Bias enabled (See Formula 3 below.)		83	93	
		Idle Mode		13	16	
		Sleep Mode		0.15	0.18	
		Servo Write Mode, All heads, VDD=5V, I_S=25mA (See Formula 4 below.)		224	250	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
V_{CC} Power Supply Current	I_{CC}	Read Mode (See Formula 5 below.)		47	56	mA
		Read Mode, Bias disabled		29	35	
		Write Mode (See Formula 6 below.)		41	50	
		Write Mode, Bias enabled (See Formula 7 below.)		48	56	
		Idle Mode (See Formula 8 below.)		18	21	
		Sleep Mode		0.34	0.40	
		Servo Write Mode, All heads, VDD=5V, I_S=25mA (See Formula 9 below.)		53	61	
Power Dissipation	P_d	Read Mode		449	577	mW
		Read Mode, Bias disabled		273	368	
		Write Mode		781	992	
		Write Mode, Bias enabled		900	1127	
		Idle Mode		194	255	
		Sleep Mode		3	4	
		Servo Write Mode, All heads, VDD=5V, I_{WS}=25mA		1387	1712	

1. IDD(Typ): 17.2 + (0.043 * I_W) + I_{MR} — IDD(Max): 20.6 + (0.046 * I_W) + (1.05 * I_{MR})
2. IDD(Typ): — IDD(Max):
3. IDD(Typ): 31.7 + (1.07 * I_W) + I_{MR} — IDD(Max): 38.0 + (1.16 * I_W) + (1.05 * I_{MR})
4. IDD(Typ): 7.77 + (10.1 * Hds) + (1.04 * I_S * Hds) — IDD(Max): 9.32 + (12.1 * Hds) + (1.12 * I_S * Hds)
5. ICC(Typ): 42.1 + (0.083 * I_W) + (0.17 * I_{MR}) — ICC(Max): 50.5 + (0.09 * I_W) + (0.18 * I_{MR})
6. ICC(Typ): — ICC(Max):
7. ICC(Typ): 39.4 + (0.18 * I_W) + (0.17 * I_{MR}) — ICC(Max): 47.3 + (0.19 * I_W) + (0.18 * I_{MR})
8. ICC(Typ): 16.5 + (0.17 * I_{MR}) — ICC(Max): 19.8 + (0.18 * I_{MR})
9. ICC(Typ): 21.9 + (1.95 * Hds) + (0.13 * I_S * Hds) — ICC(Max): 26.3 + (2.34 * Hds) + (0.14 * I_S * Hds)

I/O CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	1.5		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	-0.3		0.7	V
Input High Current	I_{IH}	Applies to SPE, SPC, SPD pins	-1		1	µA
Input Low Current	I_{IL}	Applies to SPE, SPC, SPD pins	-1		1	µA
BIASN Internal Pullup Resistor	R_{pu}	Pullup to V_{CC}	10	20	30	KΩ
R/WN Pin Internal Pullup Resistor	R_{pu}	Pullup to V_{CC}	30	50	70	KΩ
Input Signal Rise/Fall Time	t_{ir}/t_{if}	Applies to R/WN, BIASN, SPE, SPC, SPD pins			10	ns
Input Hysteresis	V_{ihys}	Applies to R/WN, BIASN, SPE, SPC, SPD pins	200			mV
Output High Current	I_{OH}	V_{OH}=3.6V, applies to FLT, SPD			1	µA
Output Low Voltage	V_{OL}	FLT I_{OL}=3mA			0.3	V
		SPD I_{OL}=5mA			0.3	
WDX/WDY Peak-to-Peak Differential Swing	V_{DS}	Write Mode	400		**TBD**	mV_{ppd}
WDX/WDY Differential Input Voltage	V_{DIFF}	Read Mode	100			mV_{diff}
		Idle Mode	0			mV_{diff}
WDX/WDY Common Mode Source Voltage	V_{CMW}		1.4	2	2.6	V
WDX/WDY Differential Input Impedance	Z_{ID}		100	125	150	Ω
WDX/WDY Input Rise/Fall Time	t_{WR}/t_{WF}	80% of V_{DIFF} into C_L=20pF		0.9	1.05	ns
RDP/RDN Differential Load Resistance	R_{LOAD}	220 Ω resistor (1%) load precedes 100pF coupling capacitors.	218	220	222	Ω
RDP/RDN Common Mode Output Voltage	V_{OCM}	Read Mode, Write Mode, BIASN = L		V_{CC} - 2.5		V
RDP/RDN Common Mode Output Voltage Difference	ΔV_{OCM}	V_{OCM} (READ) - V_{OCM} (WRITE), BIASN = L	-150		150	mV
RDP/RDN Single-Ended Output Resistance	R_{SEO}	Read Mode		30	**TBD**	Ω
RDP/RDN Output Current	I_O	Source or sink	4			mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
MR Head Current Range	I_{MR}		2	7	9.75	mA
MR Head Current Accuracy	ΔI_{MR}	2mA < I_{MR} < 9.75mA	-5		5	%
Unselected MR Head Current		Applicable **TBD** µs after head switch			10	µA
Differential Voltage Gain	A_V	V_{IN}=1mV_{pp} @80MHz, R_L(RDP, RDN)=2kΩ, applies to the following:				V/V
		4 or 6-channel VM5131B1, Gain bit=0	95	112	130	
		4 or 6-channel VM5131B1, Gain bit=1	125	150	175	
		4 or 6-channel VM5131B2, Gain bit=0	125	150	175	
		4 or 6-channel VM5131B2, Gain bit=1	160	190	220	
Gain Deviation Head-to-Head					3	%
Gain Boost	BOOST	f=80MHz, Gain bit=0, Boost bit=1		3		dB
Passband Upper Frequency Limit	f_{HR}	L_{MR}=20nH, -3dB, Gain bit=0	270	300		MHz
		-1dB, Gain bit=0	170			
Passband Lower -3dB Frequency Limit	f_{LR}	Gain bit=0	0.15	0.5	0.8	MHz
Equivalent Input Noise (sense amp only)	e_a	1 < f < 85 MHz		**TBD**		nV/√Hz
Bias Current Noise (referred to Input)	i_n			**TBD**		pA/√Hz
Equivalent Input Noise (total)	e_n	1 < f < 85 MHz		0.6	**TBD**	nV/√Hz
Integrated Noise	e_{in}	L_{MR}=20nH; 1 < f < 140 MHz		**TBD**		µV
Dynamic Range	DR	AC input V where A_V falls to 90% of its value at V_{IN}=1mV_{pp} @ f=40 MHz, Gain bit=0	10			mV_{pp}
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{DD}, 1 < f < 100 MHz	**TBD**			dB
		100 < f < 170 MHz	**TBD**			
Channel Separation	CS	Unselected Channels: V_{IN}=100mV_{pp}, 15 < f < 40 MHz	**TBD**			dB
		40 < f < 170 MHz	**TBD**			

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Noise Rejection Any I/O to RDP/RDN	NR	100 mV_{PP} on I/O, 1 < f < 225 MHz	50			dB
Output Offset Voltage	V_{OS}	Low or High Gain	-50		50	mV
Output Offset Voltage Deviation Across Heads	ΔV_{OS}				50	mV
Total Harmonic Distortion	THD	@ f = 20 MHz			**TBD**	%
DBHV Threshold (MR Head Resistance measurement)	V_{BHV}	Programmable	42		762	mV
Buffered Head Voltage Gain	A_{BHV}	VMR = 42mV - 762mV	4.75	5	5.25	V/V
Thermal Asperity Detection Range	V_{TATH}	DC level in RDX/RDY over base-line	6		762	mV_{bp}
Thermal Asperity Detection/ DBHV Threshold Tolerance	ΔV_{TATH}	DAC setting	-(10% + 3mV)		10% +3mV	mV
MR Head Voltage	V_{MR}	$I_{MR} \cdot R_{MR}$	100		900	mV
Overshoot on I_{MR} during Mode Transitions: Idle-to-Read, Write-to-Read, Head-to-Head and Bias Off-to-On	I_{MROV}	0.1V < V_{MR} < 0.9V Percent of final I_{MR}			2	%
Undershoot on I_{MR} during Mode Transitions	I_{MRUS}				0	mA

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(base to peak)	15		59.95	mA
Write Current Tolerance	ΔI_W	15mA < I_W < 59.95mA	-8		8	%
Differential Head Voltage Swing	V_{DH}	Open Head, V_{DD}=7.2V	10.8	14		V_{ppd}
		Open Head, V_{DD}=4.5V	5	8		
Unselected Head Current	I_{UH}				50	μA_{pk}
WDX/WDY Input Frequency Range	f_W		5		160	MHz
HWX/HWY Differential Output Capacitance	C_{OW}			**TBD**	**TBD**	pF
Head Current Propagation Delay	t_{D1}	From 50% points, WDX to I_W		6	15	ns
Asymmetry	A_{SYM}	Write Data has 50% duty cycle & 1ns rise/fall time			50	ps
Rise/Fall Time	t_r / t_f	10 - 90%		0.8	1.3	ns

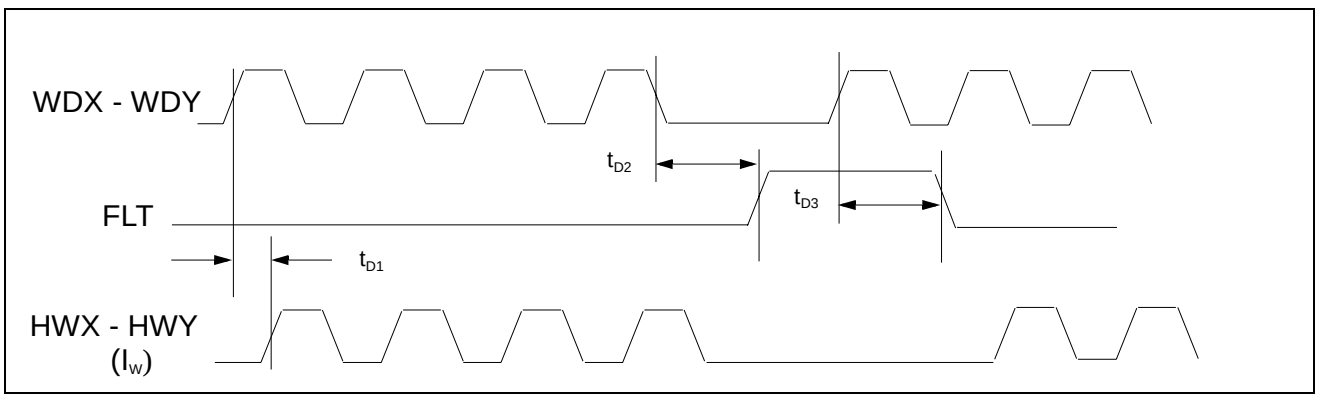


Figure 15 Write Mode Timing Diagram

Note: The write current polarity is defined by the levels of WDX and WDY (shown in the expression WDX - WDY). For WDX > WDY current flows into the “Y” port, for WDX < WDY current flows into the “X” port.

SERVO WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply	V_{CC}		4.5	5	5.5	V
	V_{DD}	LVDIS bit = 1	5		5.5	
	V_{DD}	LVDIS bit = 0	7.2		8.8	
Servo Current Range	I_S	base to peak, 6 heads	15		40	mA
		base to peak, 3 heads	15		59.95	
Servo Current Tolerance	ΔI_S	15mA < I_S < 25mA, 35mA < I_S < 59.95mA	-8		8	%
		25mA < I_S < 35mA	-5		5	
MR Head Voltage	V_{MR}	Programmable	25		226.5	mV
Read to Write Mode	t_{RW}	To 90% of servo write current		**TBD**	**TBD**	ns
Read to Write Difference between Heads		To 90% of servo write current for each head			**TBD**	ns

LOW V_{DD} OPERATION CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_S=25mA, V_{DD}=5V, LVDIS=1.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Rise/Fall Time	t_{rs}/t_{fs}	10-90%		1.75	**TBD**	ns
MR Head Current Accuracy	ΔI_{MR}	2mA < I_{MR} < 9.75mA	**TBD**		**TBD**	%
Differential Voltage Gain	A_V	V_{IN}=1mV_{pp} @80MHz, R_L(RDP, RDN)=2kW, applies to the following:				V/V
		4 or 6-channel VM5131B1, Gain bit=0	**TBD**	112	**TBD**	
		4 or 6-channel VM5131B1, Gain bit=1	**TBD**	150	**TBD**	
		4 or 6-channel VM5131B2, Gain bit=0	**TBD**	150	**TBD**	
		4 or 6-channel VM5131B1, Gain bit=0	**TBD**	190	**TBD**	
Equivalent Input Noise (total)	e_n	1 < f < 85 MHz		0.6	**TBD**	nV/$\sqrt{Hz}$
Power Supply Rejection Ratio	PSRR	100mV_{pp} on V_{CC} or V_{DD}, 1 < f < 100 MHz	**TBD**			dB
		100 < f < 170 MHz	**TBD**			
Write to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value [1]		**TBD**	**TBD**	ns

1. MRBIAS/FAST pin low for 10µs preceding R/WN transition (assumes MRB = 1 and IMR DAC).

PINNED LAYER REVERSAL CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PLR Pulse Amplitude	V_{RESET}	Referenced to ground Value set in I_W DAC (2:<D0-D4>). See (eq. 11).	0.4		1.64	V
PLR Pulse Width	t_{PW}	Value set in 7:<D2-D3>. See Table 11	50		200	ns
PLR Pulse Decay Rate	d_V/d_t	Value set in 7:<D0-D1>. See Table 12	1.75		7	mV/ns
PLR Pulse Setup Time	t_{ARM}		500			ns
PLR Pulse Delivery Time	t_{EN}		**TBD**			ns

MODE SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified: I_{MR}=8.0mA, R_{MR}=45Ω, I_W=40.0mA, L_H=85nH, R_H=12Ω, f_{DATA}=20MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Mode	t_{RW}	To 90% of write current		43	50	ns
Write to Read Mode	t_{WR}	RDP/RDN to within ±30mV of final value or 90% of read envelope [1]		180	300	ns
Idle to Read Mode [2]	t_{IR}	RDP/RDN to within ±30mV of final value or 90% of read envelope		6	10	µs
Sleep to Idle Mode [2,3]	t_{SR}	RDP/RDN to within ±30mV of final value or 90% of read envelope		**TBD**	600	µs
Read Mode, Head Select to Any Head, I_{MR} switch [2]	t_{HS}	RDP/RDN to within ±30mV of final value, or 90% of read envelope, or 90% of I_{MR}		6	10	µs
Idle Mode Powerup Time (from Sleep Mode)				300		µs
Read to Idle [2]	t_{RI}	To 10% of read envelope		0.16	0.5	µs
Write to Idle [2]	t_{WI}	To 10% of write current		**TBD**	50	ns
Read Bias Disabled to Bias Enabled	t_{RB}	BIASN pin high to low to 90% of IMR			10	µs

1. BIASN pin low for 10µs preceding R/WN transition.
2. Timing for mode change, which is initiated in serial register, is measured from SPE high to low edge.
3. Sleep to Read mode change transitions through Idle mode and must remain in Idle mode for a minimum of 300µs.

FAULT CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fault Threshold	VCC_{DTH}	I_w < 200µA, Fault detected	3.6	3.8	4.0	V
	VCC_{UTH}	Fault removed	3.9	4.1	4.3	
V_{CC} Fault Threshold Hysteresis	VCC_{HTH}		200	300	400	mV
V_{DD} Fault Threshold	VDD_{DTH}	I_w < 200µA, Fault detected	5.8	6.1	6.4	V
	VDD_{UTH}	Fault removed	6.3	6.6	6.9	
V_{DD} Fault Threshold Hysteresis	VDD_{HTH}		400	500	600	mV
Threshold for Open MR Head Fault Detection			0.95	1.1	1.3	V
Threshold for MR Head Shorted to GND Fault Detection				50		mV
Open MR Head Delay		From Head Switch to Open MR Head reported (SPE goes low to FLT pin low)		10	20	µs
Writer Open/Shorted Head Detection Threshold	V_{OSHD}	ΔV across write element at next WDX/WDY transition, where $\Delta V = R_{OpenHead} * I_W$ OR Head resistance to GND <15Ω.			2.5	V
Open/Shorted Write Head Blanking Time	t_{OS}			7 [1]		ns
FLT delay, Write Safe to Unsafe [2]	t_{D2}	Fault Safe guaranteed for write data transitions <500ns apart.	0.5	1.5	3.6	µs
FLT delay, Write Unsafe to Safe [2]	t_{D3}				1.1	µs
TA FLT Delay [3]	t_{D4}	TA detected to FLT pin low		30	100	ns
TA FLT Pulse Width [3]	t_{D5}		1	1.5	2	µs
Temperature Threshold for Hot Fault	T_{HOT}			135		°C

1. Will not detect or report fault for write current transitions less than 7ns apart.
2. See Figure 15 on page 24.
3. See Figure 5 on page 6.